Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 17. A memory device structure, comprising:
a substrate;
a tunnel oxide layer, which is disposed on the substrate;
an electron-capturing layer, which is disposed on the tunnel oxide layer;
a conductive gate layer, which is disposed on a portion of the electron-capturing layer, wherein the electron-capturing layer has a width larger than that of the conductive gate layer;
a dielectric layer, which is disposed in between the conductive gate layer and the electron-capturing layer; and
a spacer wall, which is disposed on the electron-capturing layer and on sidewalls of the conductive gate layer and the dielectric layer.

[c2] 18. The memory device structure according to claim 17, wherein the electron- capturing layer further comprises a material of silicon nitride.

[c3] 19. The memory device structure according to claim 17, wherein the spacer wall is a silicon nitride spacer wall.

[c4] 20. The memory device structure according to claim 17,

wherein the dielectric layer is made of materials including silicon oxide.

[c5] 21. The memory device structure according to claim 17, wherein the conductive gate is made of materials including poly-silicon.

[c6] 22. The memory device structure according to claim 17 further comprises a source/drain region in the substrate outside of the spacer wall.

[c7] 23. The memory device structure according to claim 17 further comprises a metal-silicon compound material layer on top of the conductive gate layer.